Amendments to the Claims:

Prior to examination of the application and calculation of the filing fee, please amend the claims as follows:

Claims 1-26 (cancelled)

Claim 27 (new): A method for level-shifting a received signal comprising:

receiving first and second input signals having voltage levels related to an external power supply voltage;

differentially comparing the first and second input signals to generate a differential current signal, wherein the differential current signal is sourced from the external power supply voltage;

providing a resistive load coupled in series with a pulling current source between an internal power supply voltage and a ground supply voltage; and

driving the resistive load with the differential current signal.

Claim 28 (new): The method of claim 27, further comprising clamping the differential current signal to the ground supply voltage.

Claim 29 (new): The method of claim 27, wherein differentially comparing the first and second input signals comprises:

driving an NMOS differential pair with the first and second input signals to obtain an intermediate differential current signal; and

reflecting the intermediate differential current signal through a PMOS current mirror pair configured to draw current from the external power supply voltage in order to generate the differential current signal.

Claim 30 (new): The method of claim 29, wherein the pulling current source is sized larger than the PMOS current mirror pair.

Claim 31 (new): The method of claim 27, wherein providing a resistive load comprises:

providing a first PMOS transistor coupled in series with a first pulling current source between the internal power supply voltage and the ground supply voltage, wherein the first PMOS transistor is configured to operate in its linear range;

providing a second PMOS transistor coupled in series with a second pulling current source between the internal power supply voltage and the ground supply voltage, wherein the second PMOS transistor is configured to operate in its linear range;

driving the first PMOS transistor with a non-inverted portion of the differential current signal; and

driving the second PMOS transistor with an inverted portion of the differential current signal.

Claim 32 (new): The method of claim 27, wherein the external power supply voltage is of a greater potential than the internal power supply voltage.

Claim 33 (new): The method of claim 27, wherein the internal power supply voltage is less than twice a transistor threshold voltage.

Claim 34 (new): The method of claim 27, wherein the first and second input signals comprise complementary data signals.

Claim 35 (new): The method of claim 27, wherein the second input signal comprises a reference voltage configured to differentiate between logic levels of the first input signal.

Claim 36 (new): A method for level-shifting a received signal comprising:

receiving first and second input signals having voltage levels related to an external power supply voltage;

differentially comparing the first and second input signals to generate a differential current signal, where the differential current signal is sourced from the external power supply voltage by:

driving an NMOS differential pair with the first and second input signals to obtain an intermediate differential current signal; and

reflecting the intermediate differential current signal through a PMOS current mirror pair configured to draw current from the external power supply voltage in order to generate the differential current signal;

providing a resistive load coupled in series with a pulling current source between an internal power supply voltage and a ground supply voltage; and

driving the resistive load with the differential current signal.

Claim 37 (new): The method of claim 36, wherein the pulling current source is sized larger than the PMOS current mirror pair.

Claim 38 (new): The method of claim 36, wherein providing the resistive load comprises:

providing a first PMOS transistor of the PMOS current mirror pair coupled in series with a first pulling current source between the internal power supply voltage and the ground supply voltage, wherein the first PMOS transistor is configured to operate in its linear range;

providing a second PMOS transistor of the PMOS current mirror pair coupled in series with a second pulling current source between the internal power supply voltage and the ground supply voltage; wherein the second PMOS transistor is configured to operate in its linear range;

driving the first PMOS transistor with a non-inverted portion of the differential current signal; and

driving the second PMOS transistor with an inverted portion of the differential current signal.